

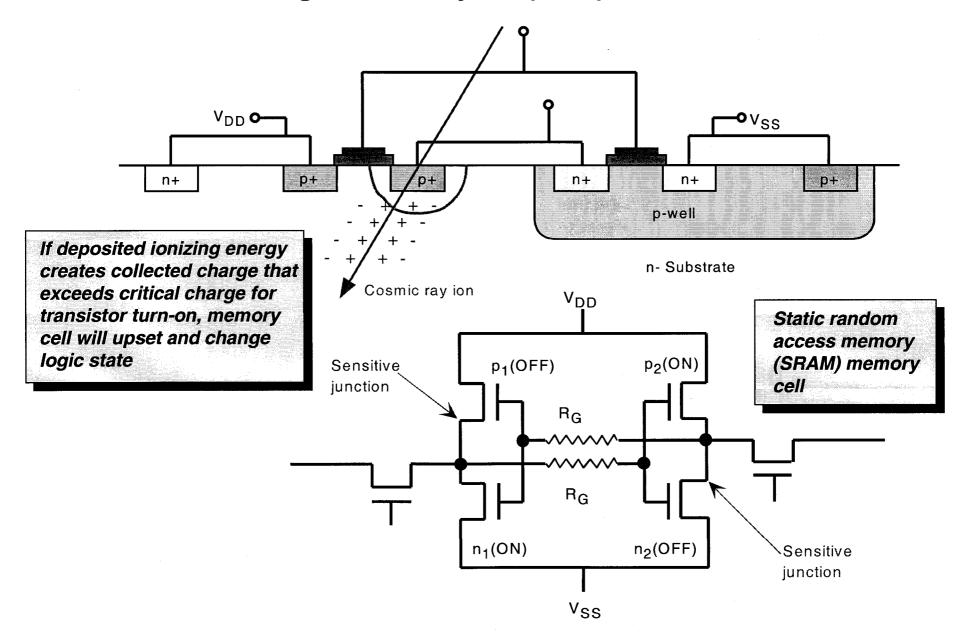


A Brief History of Memory in Space from an SEE (Single Event Effects) Perspective

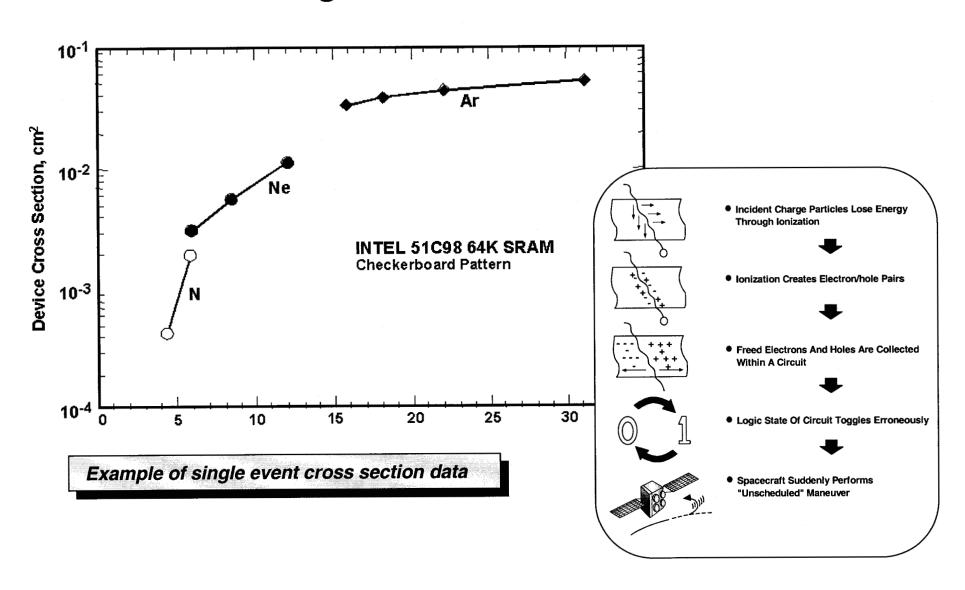
Gary Swift
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, CA

Work performed by the Jet Propulsion Lab, California Institute of Technology under contract with the National Aeronautics and Space Administration

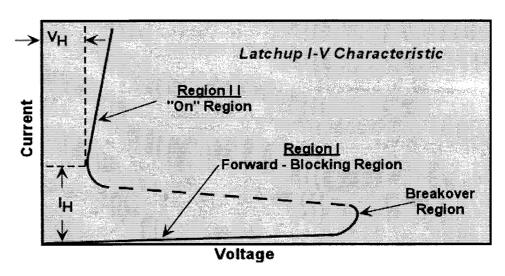
Single Event Upset (SEU) Mechanism

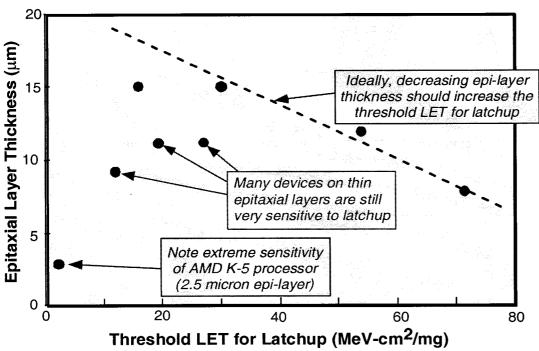


Single Event Effects



Single Event Latchup (SEL)

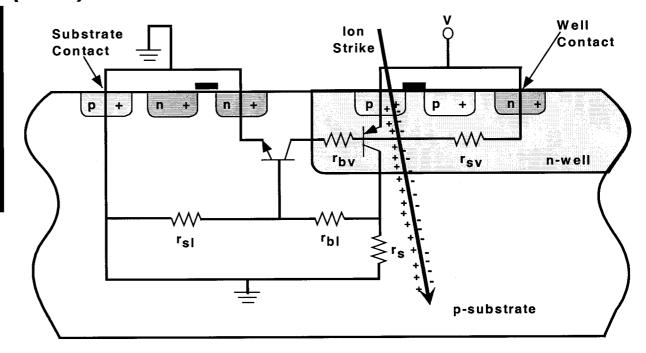




Single Event Latchup (SEL)

Initial Triggering Action:

Ion-induced current flows from well contact to substrate contact, and produces a voltage drop within the well, which, in turn, forward biases the parasitic vertical bipolar transistor



Existence of parasitic vertical and horizontal bipolar transistors (*p-n-p-n*) allows regenerative structure to exist and makes circuit susceptible to latchup

When the product of the gains of these transistors is greater than 1, an SCR-like action takes place and latchup can occur

Notes:

Definition of SEE: An observable electrical disturbance from an individual ionizing particle strike

Use of "pure" commercial devices is increasing because:

- Most rad-hard foundries have closed
- •Commercial devices are more attractive to designers, more dense and lower power

Use of commercial devices is possible because:

- Variety of mfrs. increase the chance of finding a fortuitously rad-hard device
- •VLSI makes viable complex error correction circuitry

Bipolar SRAM ICs and Early CMOS SRAMs

Examples:

93L422 2k bits - many missions incl. Topex/Poseidon CD4061 256 bits - Voyager

SEEs:

Cell upsets

Rad-hard CMOS SRAMs

Examples:

TCC244 1k bits (Sandia foundry) - Galileo

6516 16k bits (Harris foundry) - Magellan

SEEs:

Cell upsets

Latchup (fixed by rad-hard foundries)

Micro-dose stuck bits

DRAMs

Examples: MSM514400 4Mb DRAMs - Cassini

Luna-C,-E 16Mb DRAMs - Pathfinder, Seawinds,...

SEEs: Cell upsets - error correcting circuitry fixes

Multiple bit upset

Stuck bits

Problematic for ECC

Latchup - by luck, some mfrs. immune

Functional interrupts

Flash Memory

Examples: KM 29U128 128Mbit

- X2000: Europa Orbiter, Solar Probe, Pluto/Kuiper Express

SEEs:

State Machine Upsets Lockups Block destruction

Earlier...

Core Magnetic Memory

Examples:

Plated Wire - Viking I & II

SEEs:

None!

Further Out...

Advanced Non-Volatile Technologies (?)

Possibilities:

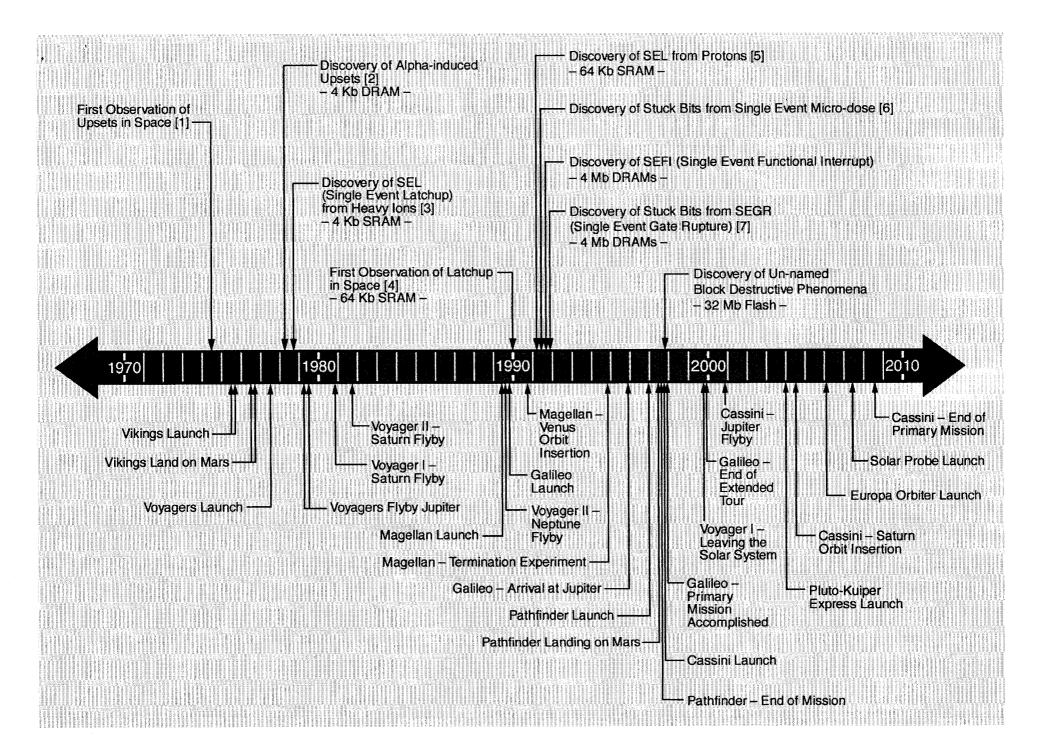
Ferro-electric RAMs - sets and senses dielectric polarization

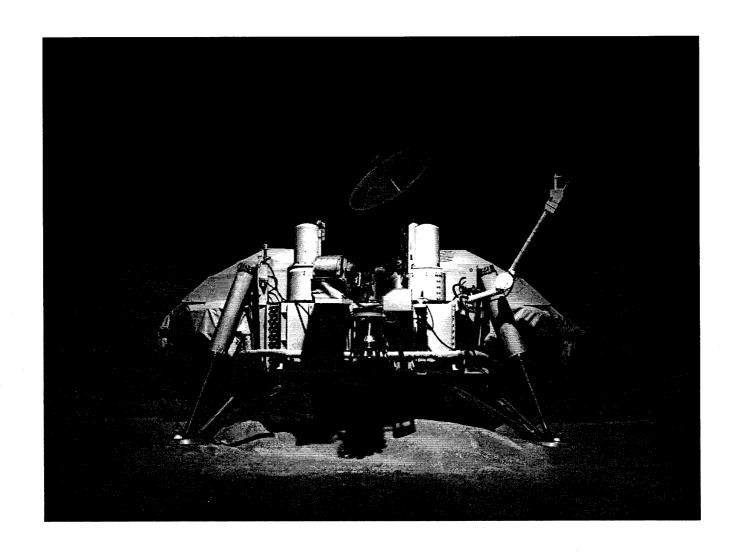
GMR (Giant Magneto-resistive) RAMs

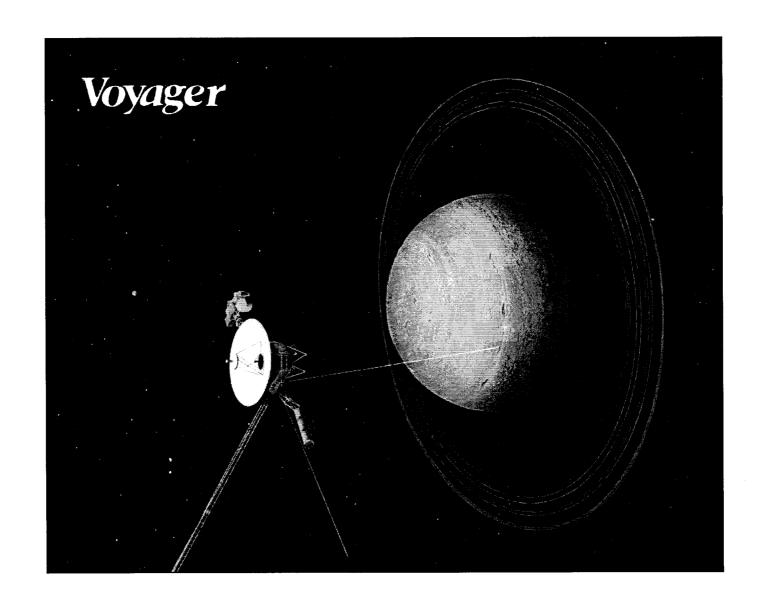
C-RAM (based on chalcogenide)

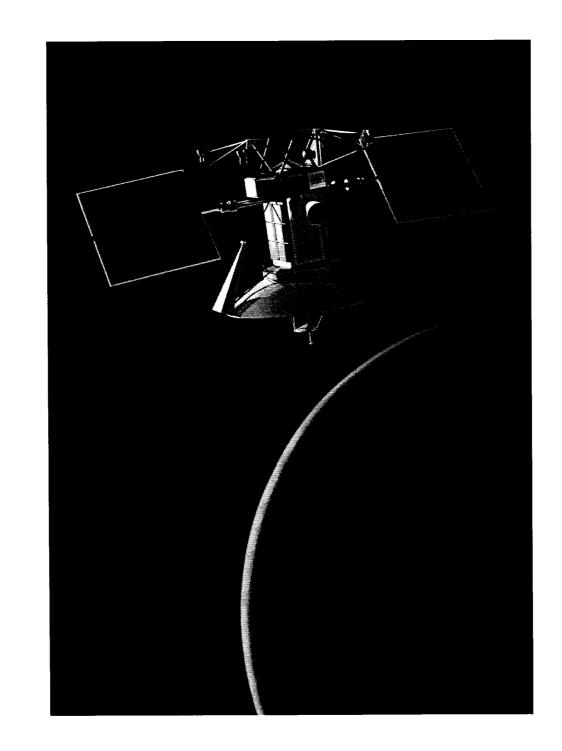
SEEs:

To be found

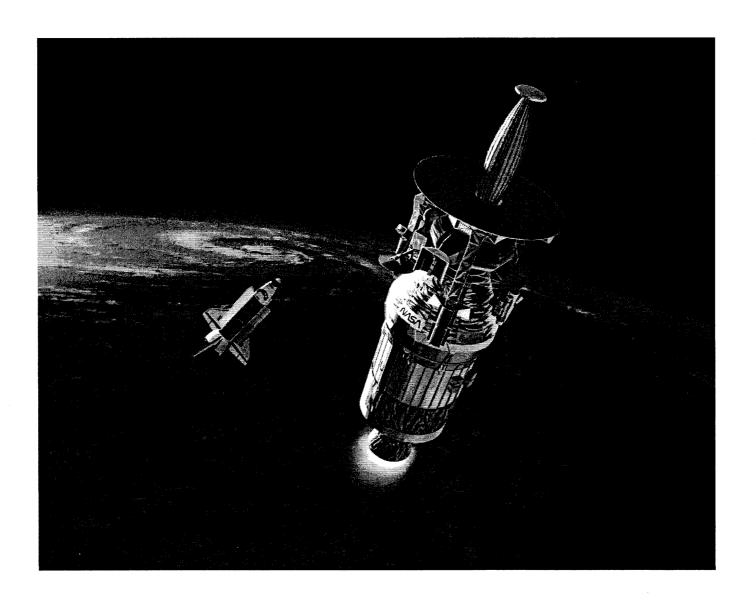






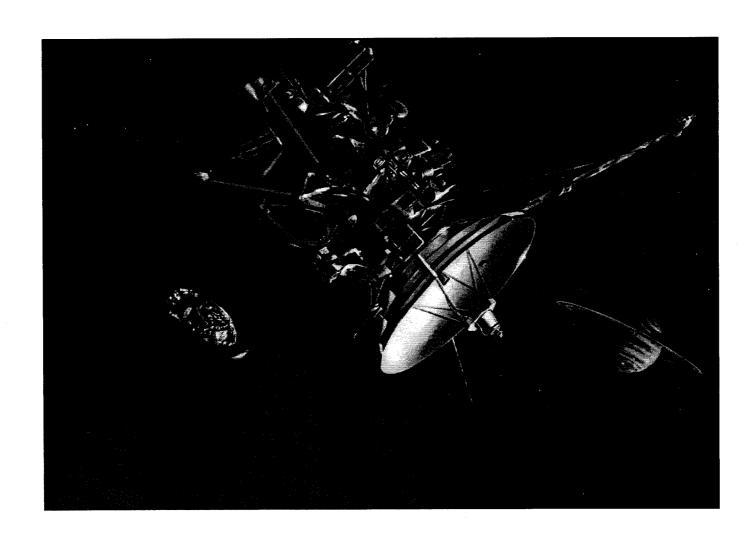


· 1



× 1









References:

- [1] D. Binder, et al., "Satellite Anomalies from Galactic Cosmic Rays", *IEEE Trans. Nucl. Sci.*, v. 22, p. 2675 (1975)
- [2] T.C. May & M.H. Woods, "Alpha-Particle-Induced Soft Errors in Dynamic Memories", *IEEE Trans. Elec. Dev.*, v. 26, p. 2 (1979)
- [3] T. Goka, et al., "The On-Orbit Measurements of Single Event Phenomena by ETS-V Spacecraft", *IEEE Trans. Nucl. Sci.*, v. 38, p. 1693 (1991)
- [4] W.A. Kolasinski, et al., "Simulation of Cosmic Ray Induced Soft-errors and Latchup in Integrated Circuit Computer Memory", *IEEE Trans. Nucl. Sci.*,v. 26, p. 5087 (1979)
- [5] D.K. Nichols, et al., "An Observation Of Proton-Induced Latchup", *IEEE Trans. Nucl. Sci.*, v. 39, p. 1654 (1992)
- L. Adams, et al., "A Vertical Proton Induced Latchup in Space", *IEEE Trans. Nucl. Sci.*, v. 39, p. 1009, (1992)
- [6] C. Dufour, et al., "Heavy Ion Errors on Submicronic Memories", *IEEE Trans. Nucl. Sci.*, v. 39, p. 1693 (1992)
- [7] G. Swift, et al., "A New Class Of Single Event Hard Errors", *IEEE Trans. Nucl. Sci.*, v. 41, p. 2043 (1994)